#14 Appeal Brief 11-14-03 L. Sprunell

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of
OHMINAMI, Nobuyuki
Serial No. 10/003,258
Filed: December 6, 2001

Atty. Ref.: 829-593
Group: 2854
Examiner: Hamdan, Wasseem

For: APPARATUS AND METHOD FOR ANALYZING CAPACITANCE OF INSULATOR

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November 10, 2003

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

Applicant hereby appeals the Final Rejection of April 8, 2003, Paper No. 6.

REAL PARTY IN INTEREST

The real party in interest is Sharp Kabushiki Kaisha, a corporation of the country of Japan.

RELATED APPEALS AND INTERFERENCES

The appellant, the undersigned, and the assignee are not aware of any related appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 1-10 are pending. Claims 1-3 and 5-9 have been rejected; while claims 4 and 10 have been allowed as indicated in the Advisory Action dated October 21, 2003. Thus, only the rejected claims (i.e., claims 1-3 and 5-9) are on appeal herein.

STATUS OF AMENDMENTS AFTER FINAL

Two (2) separate "after final" filings have been submitted – both have been considered and entered. In particular, the Amendment After Final dated October 7, 2003 has been *entered* as indicated by the Advisory Action dated October 21, 2003; and the Response After Final dated July 2, 2003 has also been considered/entered as indicated by the Advisory Action dated July 22, 2003.

By way of the Response After Final filed/dated July 2, 2003, the drawing objection has been overcome. See the Advisory Action dated July 22, 2003. The Amendment After Final dated October 7, 2003 merely placed "objected to" claims 4 and 10 in independent form so that they are now allowed as indicated by the Advisory Action dated October 21, 2003.

SUMMARY OF EXAMPLE EMBODIMENTS OF INVENTION

The instant invention relates to an insulator capacitance analyzer for analyzing C-V characteristics of an electronic structure, and methods relating to the same.

For background purposes, Kono (i.e., JP 6-112289 used by the Examiner in the final rejection) is discussed in the Background section of the instant application at pages 5-7 as indicative of the prior art (see also prior art Fig. 9 of the instant application). Kono

discloses a single MAIS (Metal/Air/Insulator/Semiconductor) structure, where a *non-contact* type analyzer is spaced apart from the structure to be analyzed via an air gap. In particular, Kono's metal layer (M in MAIS) is spaced apart from the insulator (I in MAIS) of the MAIS to be measured via an air gap (A in MAIS).

A primary problem with the prior art (exemplified by Kono) stems from the fact that it requires measurement of an insulator in a *non-contacting* relation (see pg. 5, line 16 to pg. 6, line 5 of the instant specification). In other words, there is a space (air gap with a capacitance C_{air}) between the contactless measuring device of Kono and the insulator to be measured. This non-contacting measuring used by Kono is problematic in that it causes errors to occur because the precise spacing required between the measuring device and the insulator cannot be sufficiently controlled and dust therebetween may lead to short-circuiting (see pg. 6, line 12 to pg. 7, line 8 of the instant specification). Moreover, another significant problem with Kono is that its non-contacting measuring device can only be used immediately after the insulator has been formed (*before* the metal has been formed thereover to form the MIS) – this prevents the device of Kono from being able to efficiently analyze boron punch-through in a MIS which is a significant need in the art (see pg. 7, lines 8-15 of the instant specification). Thus, it can be seen that the contactless measuring requirement of Kono leads to many problems.

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Such problem(s) are solved by the instant invention. For purposes of example and without limitation, Figs. 1-2 of the instant application illustrate that certain embodiments of this invention relate to an insulator capacitance analyzer 10 including a capacitance structure 1 having known capacitance C1. The capacitance structure 1 may comprise any MIS (Metal/Insulator/Semiconductor) structure such as a MOS

(Metal/Oxide/Semiconductor), or any other suitable type of capacitance structure. The known capacitance C1 is serially connected to a MIS structure 2 (referred to in certain claims as a first MIS structure) to be measured. The MIS structure 2 to be analyzed has an unknown capacitance C_2. A measuring section (e.g., LCR) 3 is provided for measuring synthesis capacitance of the serially-connected MIS structure 2 and capacitance structure 1.

In contrast with conventional art such as Kono, certain example embodiments of this invention provide for an analyzing device capable of creating a serial connection between the capacitance structure 1 with known capacitance and the MIS to be measured. This is highly advantageous in that it enables a MIS structure to be measured (after the metal has been formed over the insulator – which is not possible in Kono) so that boron punch-through or the like can be analyzed (e.g., pg. 18, lines 9-20 of the instant specification). The conventional short-circuiting problem realized by Kono is also overcome due to the use of the serial connection between the capacitance structure and the MIS to be measured.

When using the serial connection of certain example embodiments of the instant invention, even when an insulator of the MIS is thin so that direct tunnel leakage current flows through the MIS structure, excessive leakage can be prevented from flowing through an insulator capacitance analyzer so long as the capacitance structure is structured such that the direct tunnel leakage current cannot flow therethrough (i.e., the capacitance structure is dominated by F-N tunnel leakage current). Therefore, the synthesis capacitance can be accurately measured. It is also possible to analyze effects on capacitance caused by boron ions punching through the P+ electrode in the MIS

structure having a thin insulator. Thus, C-V characteristics of an extremely thin insulator can be accurately measured without being affected by direct tunnel leakage current, and boron ions punching through a P+ electrode in a MIS structure can be analyzed (e.g., pg. 9, line 19 to pg. 11, line 6).

Thus, it is possible according to certain example embodiments of this invention to accurately measure a synthesis capacitance of a MIS structure to which a capacitance structure having known capacitance is serially connected. The unknown capacitance is calculated from the synthesis capacitance. Accordingly, C-V characteristics of a MIS structure can be more efficiently analyzed (e.g., pg. 24, line 22 to pg. 25, line 18).

ISSUES

1. Whether claims 1-3 and 7-9 are anticipated under 35 U.S.C. Section 102(b) by Kono (JP 6-112289).

2. Whether claims 5-6 are unpatentable under 35 U.S.C. Section 103(a) over Kono in view of Oki (JP 11-150246).

GROUPING OF CLAIMS

The appealed claims are divided into the following separate and distinct groups.

Group A: claims 1-3

Group B: claims 5-6

Group C: claim 7

Group D: claims 8-9

Each of the aforesaid groups is patentably distinct from the other groups. For example, claim 7 does not stand/fall together with any other claim. As another example, claims 1-3 stand/fall together, but do not stand/fall together with any other claim(s).

ARGUMENT

It is axiomatic that in order for a reference to anticipate a claim, it must disclose, teach or suggest each and every feature recited in the claim. See, e.g., Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983). The USPTO has the burden in this respect.

Moreover, the USPTO has the burden under 35 U.S.C. Section 103 of establishing a *prima facie* case of obviousness. In re Piasecki, 745, F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). It can satisfy this burden only by showing that some objective teaching in the prior art, or that knowledge generally available to one of ordinary skill in the art, would have led that individual to combine the relevant teachings of the references to arrive at the claimed invention. In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Before the USPTO may combine the disclosures of the references in order to establish a *prima facie* case of obviousness, there must be some suggestion for doing so. In re Jones, 958 F.2d 347 (Fed. Cir. 1992). Even assuming, *arguendo*, that a given combination of references is proper, the combination of references must in any event disclose all features of the claimed invention in order to render it obvious.

Group A: Claim 1 (together with which claims 2-3 stand/fall)

Claim 1 stands rejected under 35 U.S.C. Section 102(b) as being allegedly anticipated by Kono (JP 06-112289). This Section 102(b) rejection should be reversed for at least the following reasons.

Claim 1 requires "a capacitance structure having known capacitance and configured so as to be serially connectable to the first MIS structure; and a measuring section for measuring synthesis capacitance of the serially-connected first MIS structure and capacitance structure." For example, Fig. 1 of the instant application illustrates that capacitance structure 1 with a known capacitance C1 and MIS structure 2 to be measured are *serially connected* to one another; and the LCR meter 3 functions as a measuring section in order to measure synthesis capacitance of the *serial connected* structures 2 and 3. This serially connected structures are highly advantageous, for example, in that they allows C-V characteristics of an extremely thin insulator to be accurately measured without being adversely affected by directly tunnel leakage current, and boron ions punching through an electrode in the MIS structure can also be analyzed. The cited art fails to disclose or suggest at least the aforesaid underlined aspects of claim 1.

In contrast to claim 1, Kono merely discloses a single MAIS (Metal/Air/Insulator/Semiconductor) structure, where a *non-contact* type analyzer is spaced apart from the structure to be analyzed via an air gap. In particular, Kono's metal layer (M in MAIS) is spaced apart from the insulator (I in MAIS) of the MAIS to be measured via an air gap (A in MAIS). Because Kono merely discloses this single MAIS structure, it cannot possibly disclose or suggest a capacitance with known capacitance serially connected to a MIS structure as required by claim 1.

Kono, and the problems associated therewith, are discussed on pages 5-7 of the instant specification. The primary problem with Kono stems from the fact that it requires measurement of an insulator in a *non-contacting* relation (see pg. 5, line 16 to pg. 6, line 5 of the instant specification). In other words, there is a space (air gap with a capacitance C_{air}) between the contactless measuring device of Kono and the insulator to be measured. This non-contacting requirement of Kono is problematic in that it causes errors to occur because the precise spacing required between the measuring device and the insulator cannot be sufficiently controlled and dust therebetween may lead to short-circuiting (e.g., pg. 6, line 12, to pg. 7, line 8, of the instant specification). Another significant problem with Kono is that its non-contacting measuring device can only be used immediately after the insulator has been formed (*before* the metal has been formed thereover to form the MIS) – this prevents the device of Kono from being efficiently used to analyze boron punch-through which is a significant need in the art (e.g., pg. 7, lines 8-15, of the instant specification). Accordingly, it can be seen that the contactless requirement (non-serial-connection) of Kono leads to many problems.

In contrast with Kono which merely discloses a single MAIS structure using an air gap, the invention of claim 1 eliminates the air gap and the problems associated therewith by using a serial connection between a capacitance structure having known capacitance and a MIS to be measured. This is highly advantageous in that it allows a MIS structure to be measured (*after* the metal has been formed over the insulator) so that boron punch-through can be analyzed (e.g., pg. 18, lines 9-20, of the instant specification). The short-circuiting problem of Kono may also be overcome. Kono is not even capable of

measuring a MIS structure, let alone providing a serial connection between such a structure and a capacitance structure with known capacitance.

In contrast with claim 1, Kono discloses a single MAIS where the metal electrode (M in MAIS) is spaced apart from the insulator (I in MAIS) of the MAIS to be measured via an air gap (A in MAIS). The spacing of a metal M from an insulator I with an air gap A therebetween in Kono does not represent a serial connection between the metal and the insulator, let alone a serial connection between a MIS and a capacitance structure with known capacitance as required by claim 1.

According, it can be seen that Kono fails to disclose or suggest the serially-connected MIS and capacitance structure of claim 1. Instead, the reference teaches directly away from this by requiring a contactless relation between a metal and an insulator, so that the insulator must be analyzed before a metal if formed thereon (i.e., before a MIS is formed). Claim 1 is not anticipated, and the reference is entirely unrelated to the invention thereof.

Furthermore, contrary to the Examiner's contention, Kono's V_{fbMAIS} is not a capacitance structure with known capacitance. Kono discloses a single MAIS structure (the MIS is an ideal or imagined structure calculated from measurements performed on the MAIS). Drawing 2 of Kono merely shows an equivalent circuit of the device when flat band voltage (V_{fbMAIS}) is taken into account; i.e., the device still includes a single MAIS structure. The flat band voltage (V_{fbMAIS}) of Kono is not a capacitance structure at all. Thus, the Examiner's contention that V_{fbMAIS} is a capacitance structure with known capacitance is wrong. Since V_{fbMAIS} in Kono is not even a capacitance structure with known capacitance, the reference cannot possibly disclose or suggest a capacitance

structure serially connected to a MIS as required by claim 1. The single MAIS of Kono cannot have a capacitance structure with known capacitance serially connected to a MIS as required by claim 1. Kono is entirely unrelated to the invention of claim 1. The fundamental basis of the rejection is based on an incorrect interpretation of the cited reference by the Examiner. It can be seen that the Section 102(b) rejection is incorrect for this reason in addition to the reason discussed above.

Additionally, as explained above, the MIS structure of Kono is hypothetical and calculated from the measurements performed on the MAIS structure. In other words, Kono discloses using a Metal/Air/Insulator/Semiconductor (MAIS) structure – but not directly analyzing any MIS structure. In this respect, Kono determines measurements using a MAIS, and then uses these measurements to approximate what characteristics would be of a *hypothetical* MIS. This is because, as explained above, Kono's device is not capable of analyzing a MIS structure. Accordingly, it can be seen that, contrary to claim 1, the device of Kono is not for analyzing C-V characteristics of a MIS structure having unknown capacitance. Furthermore, since Kono is actually measuring a MAIS (not a MIS), there cannot possibly be any serial connection to a MIS or measuring synthesis capacitance of a MIS as required by claim 1. The Section 102 anticipation rejection is incorrect for this additional reason as well.

Group B: Claims 5-6

Claims 5-6 stand rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Kono in view of Oki (JP 11-150246). This Section 103(a) rejection should be reversed for at least the following reasons.

Claim 5 requires that "the equivalent silicon oxide thickness of the capacitance of the capacitance structure is 3 nm or more." Claim 6 requires that the capacitance structure is configured so as to prevent direct tunnel leakage current from flowing through the capacitance structure.

The Examiner admits that Kono fails to disclose or suggest these aspects of claims 5-6. Recognizing these deficiencies, the Examiner cites Oki. However, unlike Kono, Oki does not relate to a capacitance analyzer. Instead, Oki merely relates to a SiN/SiO/SiN layer stack used in a semiconductor device capacitor on a substrate – not an analyzer. The two references are unrelated to one another. There is no suggestion present in the art which would have caused one of skill in the art to have used Oki's three layer stack of SiN/SiO/SiN in Kono's MAIS. In fact, Oki teaches directly away from use in an analyzer circuit since the structure of Oki is provided on a substrate 1. There is no disclosure or suggestion that leakage current is a problem in Kono, especially because Kono is a non-contact type device. The Examiner has thus not met his burden of proving a *prima facie* case of obviousness, due to a lack of suggestion or motivation in the cited art. Furthermore, the

Group C: Claim 7

Claim 7 stands rejected under 35 U.S.C. Section 102(b) as being allegedly anticipated by Kono. This Section 102(b) rejection should be reversed for at least the following reasons.

Claim 7 requires "serially connecting the first MIS structure to a capacitance structure having known capacitance; measuring synthesis capacitance of the serially connected first MIS structure and capacitance structure; and calculating capacitance of

the first MIS structure based on the synthesis capacitance." For example, see the instant specification at page 18, line 14 to page 19, line 4; and also Fig. 4.

As explained above, Kono fails to disclose or suggest serially connecting a capacitance with known capacitance to a MIS to be measured as required by claim 7. Kono discloses only a single MAIS, which cannot possibly represent a MIS serially connected to a capacitance with known capacitance. For this reason, the claim cannot be anticipated.

Contrary to the Examiner's contention, Kono's V_{fbMAIS} is not a capacitance structure with known capacitance. Kono discloses a single MAIS structure (the MIS is an ideal or imagined structure calculated from measurements performed on the MAIS). Drawing 2 of Kono merely shows an equivalent circuit of the device when flat band voltage (V_{fbMAIS}) is taken into account; i.e., the device still includes a single MAIS structure. The flat band voltage (V_{fbMAIS}) is not a capacitance structure at all – it is represented in Drawing 2 of Kono as two cells in series. Thus, the Examiner's contention that V_{fbMAIS} is a capacitance structure with known capacitance is clearly wrong. Since V_{fbMAIS} in Kono is not even a capacitance structure with known capacitance, the reference cannot possibly disclose or suggest a capacitance structure with known capacitance serially connected to a MIS as required by claim 7 (i.e., the single MAIS of Kono cannot have a capacitance structure with known capacitance serially connected to a MIS as required by claim 7). The fundamental basis of the rejection is based on an incorrect interpretation of the cited reference by the Examiner. It can be seen that the Section 102(b) rejection is incorrect.

Furthermore, the measured structure in Kono is a MAIS, not a MIS. Kono's MIS is hypothetical. Thus, Kono never even measures synthesis capacitance of a MIS structure, let alone that of a MIS structure serially connected to a capacitance structure. This is because, as explained above, Kono's device is not capable of analyzing a MIS structure. Claim 7 cannot be anticipated for this reason as well.

For at least these reasons, claim 7 cannot be anticipated by Kono; the rejection thereof should be reversed.

Group D: Claim 8 (together with which claim 9 stands/falls)

Claim 8 stands rejected under 35 U.S.C. Section 102(b) as being allegedly anticipated by Kono. This Section 102(b) rejection should be reversed for at least the following reasons.

Claim 8 requires an "insulator capacitance analyzer for analyzing C-V characteristics of a first MIS (Metal/Insulator/Semiconductor) structure, comprising: a capacitance structure having a known capacitance and serially connected to the first MIS structure; and a measuring section for measuring a synthesis capacitance of the serially-connected first MIS structure and the capacitance structure."

As explained above, the single MAIS of Kono cannot possibly disclose or suggest a MIS serially connected to a capacitance structure with known capacitance. Claim 8 cannot be anticipated for at least this reason.

Furthermore, the measured structure in Kono is a MAIS, not a MIS. Kono's MIS is hypothetical. Thus, Kono never even measures synthesis capacitance of a MIS structure, let alone that of a MIS structure serially connected to a capacitance structure.

This is because, as explained above, Kono's device is not capable of analyzing a MIS structure. Claim 8 cannot be anticipated for this reason as well.

For at least these reasons, claim 8 cannot be anticipated by Kono; the rejection thereof should be reversed.

CONCLUSION

In conclusion, it is believed that the application is in clear condition for allowance; therefore, early reversal of the Final Rejection and passage of the subject application to issue are earnestly solicited.

Respectfully submitted,

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APPENDIX

CLAIMS ON APPEAL

1. An insulator capacitance analyzer for analyzing C-V characteristics of a first MIS structure having unknown capacitance, comprising:

a capacitance structure having known capacitance and configured so as to be serially connectable to the first MIS structure; and

a measuring section for measuring synthesis capacitance of the serially-connected first MIS structure and capacitance structure.

2. An insulator capacitance analyzer according to claim 1, wherein the capacitance structure includes at least one of a second MIS structure, a dielectric, and a capacitor.

3. An insulator capacitance analyzer according to claim 1, wherein the capacitance structure is configured so as to be removable from the insulator capacitance analyzer.

4. (Allowed)

5. An insulator capacitance analyzer according to claim 1, wherein the equivalent silicon oxide thickness of the capacitance of the capacitance structure is 3 nm or more.

6. An insulator capacitance analyzer according to claim 1, wherein the capacitance structure is configured so as to prevent direct tunnel leakage current from flowing through the capacitance structure.

7. An insulator capacitance analysis method for analyzing C-V characteristics of a first MIS structure having unknown capacitance, comprising the steps of:

serially connecting the first MIS structure to a capacitance structure having known capacitance;

measuring synthesis capacitance of the serially connected first MIS structure and capacitance structure; and

calculating capacitance of the first MIS structure based on the synthesis capacitance.

8. An insulator capacitance analyzer for analyzing C-V characteristics of a first MIS (Metal/Insulator/Semiconductor) structure, comprising:

a capacitance structure having a known capacitance and serially connected to the first MIS structure; and

a measuring section for measuring a synthesis capacitance of the serially-connected first MIS structure and the capacitance structure.

9. The insulator capacitance analyzer of claim 8, wherein the capacitance structure includes at least one of a second MIS structure, a dielectric and a capacitor.

10. (Allowed)